03500.017437. PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	:	Examiner: Craig Thompson
TAKESHI TAKADA, ET AL.	)	
	:	Group Art Unit: 2813
Application No.: 10/626,656	)	
	:	
Filed: July 25, 2003	)	
	:	
For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING SAME	)	
	:	
	)	March 14, 2005

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attention Docket Clerk: Code REAS

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Sir:

Applicants are in receipt of a Notice of Allowance dated December 14, 2004, in the above-referenced application. The issue fee is due on March 14, 2005, and is being paid concurrently herewith.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on

March 14, 2005
(Date of Deposit)

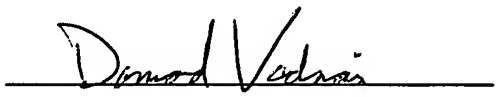
Damond E. Vadnais, Reg. No. 52,310
(Name of Attorney for Applicant)

Damond Vadnais — **March 14, 2005**
Signature — **Date of Signature**

Applicants respectfully traverse the Reasons for Allowance set forth in the Notice of Allowability on the grounds that contrary to the Reasons, Claim 20 does not recite "a second transparent layer is also formed on the second semiconductor layer and passivation treatments are carried out on the defects in the first semiconductor layer before the formation of the second semiconductor layer as well as on the second semiconductor layer."

Applicants' undersigned attorney may be reached in our Costa Mesa, California office at (714) 540-8700. All correspondence should continue to be directed to our below-listed address.

Respectfully submitted,



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